Addendum

MPC8260AUMAD/D
Rev. 0.1, 2/2002

MPC8260 PowerQUICC II™ User's Manual: MPC8260A (HiP4) Supplement

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This document describes implementation of the MPC8260A—the HiP4-process technology version of the MPC8260 PowerQUICC II microprocessor—and differences between the MPC8260A the MPC8260 (HiP3 version). All of the information in the *MPC8260 PowerQUICC II User's Manual* (which applies to the HiP3 process) also applies to the MPC8260A with the exceptions and additions noted in this document. In the event information in the two documents conflict, information presented here supersedes that in the *MPC8260 PowerQUICC II User's Manual*.

NOTE

Section, table, and figure numbering in this document indicates the chapter in the *MPC8260 PowerQUICC II User's Manual* to which each item corresponds. HiP4 additions and changes do not pertain to all chapters; therefore, not all chapters are referred to in this document.

A revision history of this document is provided at the end.

MPC826*x*A Devices and Documentation

Motorola offers four HiP4-enhanced derivatives of the MPC8260 PowerQUICC II family. Table 1 shows the functionality that defines each derivative.

Table 1. HiP4 MPC826*x*A PowerQUICC II Family Derivatives

Functionality	Derivatives			
	MPC8260A	MPC8264A	MPC8265A	MPC8266A
HiP4 Process Enhancements	X	X	X	X
PCI Bridge			X	X
Transmission Convergence (TC) Layer		X		X
Inverse Multiplexing for ATM (IMA)		X		X

Until the current *MPC8260 PowerQUICC II User's Manual* (Rev 0) is updated, several addendum documents like this one supply information about the functionality of HiP4-enhanced PowerQUICC II devices. Table 2 lists each device and its related documentation.

Table 2. HiP4 PowerQUICC II Documentation[1]

Document	Derivatives			
	MPC8260A	MPC8264A	MPC8265A	MPC8266A
MPC8260 PowerQUICC II User's Manual, Rev 0 (Document order number: MPC8260UM/D)	X	X	X	X
Errata to the MPC8260 PowerQUICC II User's Manual (Document order number: MPC8260UMAD/D)	X	X	X	X
MPC8260A (HiP4) Supplement to the MPC8260 PowerQUICC II User's Manual (Preliminary) (Document order number: MPC8260AUMAD/D)	X	X	X	X
PCI Bridge Functional Specification (Preliminary) (Document order number: MPC8265AUMAD/D)			X	X
TC Layer Functional Specification (Preliminary) (Document order number: MPC8264AUMAD/D)		X		X
IMA Functional Specification (Preliminary) (Document order number: MPC8266AUMAD/D)		X		X

[1] These documents are available at www.motorola.com/semiconductors.

Overview (Chapter 1)

This section summarizes new features of the MPC8260A (see Figure 1-1).

1.1 Features

The major additional features of the MPC8260A are as follows:

- Major new CPM features:
  - 32-Kbyte dual-port RAM
  - Additional MCC host commands

1.2 MPC826xA Architecture Overview

Figure 1-1 shows the block diagram for the MPC8266A, the superset device.

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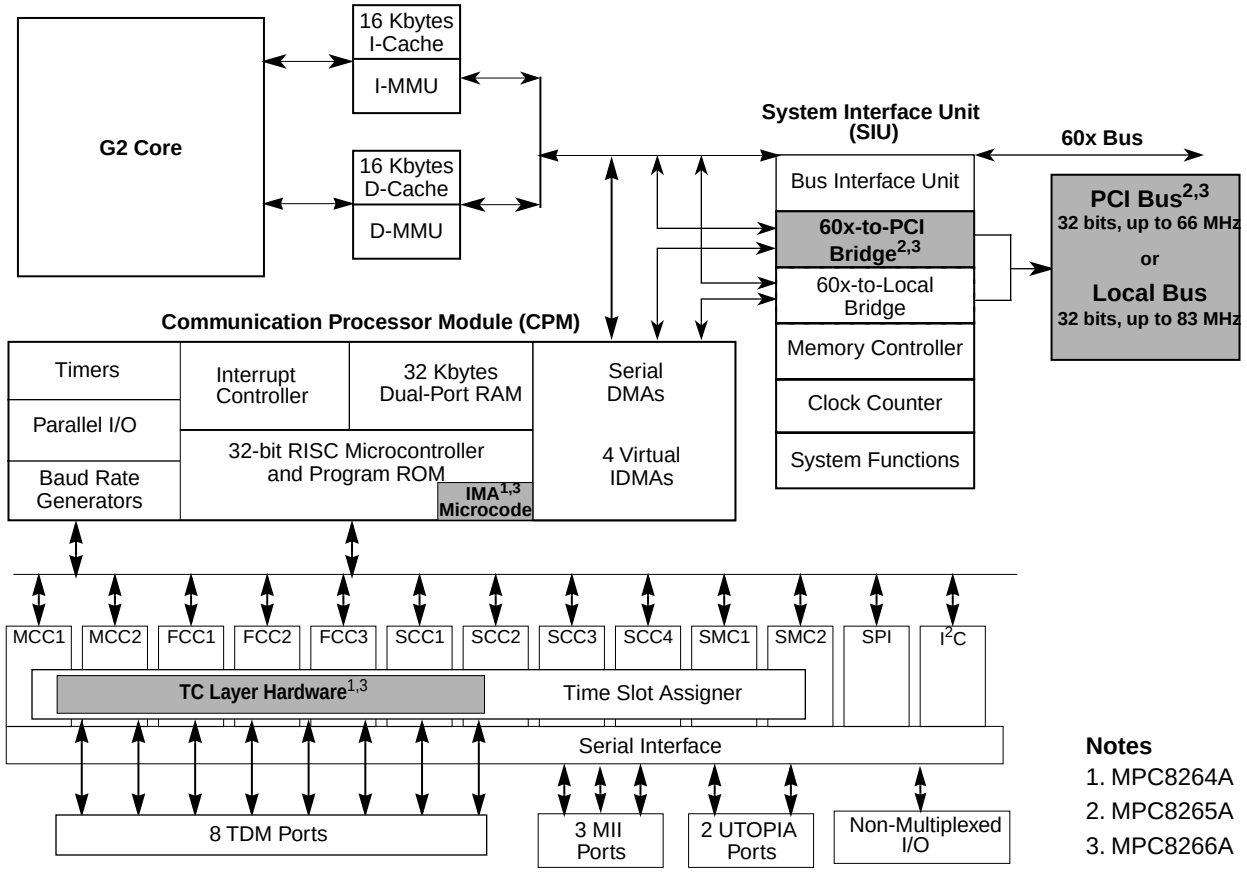

Figure 1-1 MPC826xA Block Diagram

Memory Map (Chapter 3)

Table 3-1 shows the HiP4 additions to the internal memory map of the MPC8260A. Note that PCI and TC layer portions of the memory map can be found in separate documentation (see Table 2).

Table 3-1. Additions to the Internal Memory Map

Internal Address	Abbreviation	Name	Size	Section/Page Number
CPM Dual-Port RAM				
04000–05FFF	DPRAM	Dual-port RAM (microcode only)	8 Kbytes	—
06000–07FFF	Reserved	—	8 Kbytes	—
General SIU				
Same as *MPC8260 Power QUICC II User's Manual*				
Memory Controller				
Same for MPC8260A. For PCI registers, refer to the *PCI Bridge Functional Specification* (see Table 2).				
System Integration Timers				
Same				

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Table 3-1. Additions to the Internal Memory Map (Continued)

Internal Address	Abbreviation	Name	Size	Section/Page Number
Interrupt Controller				
Same				
Clocks and Reset				
Same				
Input/Output Port				
Same				
CPM Timers				
Same				
SDMA–General				
Same				
IDMA				
Same				
FCCs				
Same				
TC Layers				
Refer to the *TC Layer Functional Specification* (see Table 2).				
BRGs 5–8				
Same				
I^2C				
Same				
Communications Processor				
Same				
BRGs 1–4				
Same				
SCCs				
Same				
SMCs				
Same				
SPI				
Same				
CPM Mux				
Same				

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Table 3-1. Additions to the Internal Memory Map (Continued)

Internal Address	Abbreviation	Name	Size	Section/Page Number
SI1 Registers				
Same				
MCC1 Registers				
Same				
SI2 Registers				
Same				
MCC2 Registers				
Same				
SI*x* RAM				
Same				

System Interface Unit (SIU) (Chapter 4)

The MPC8260A SIU is the same as the HiP3 version with the exception of fields that have been added to the bus transfer error status and control registers (TESCR1 and L_TESCR1). These additions are described in the following sections.

The interrupt priorities of the PCI bridge (MPC8265A and MPC8266A only) and TC layer (MPC8264A and MPC8266A only) are also programmed in the SIU. For descriptions of the additional register fields related to the PCI bridge and the TC layer, refer to the *PCI Bridge Functional Specification* and the *TC Layer Functional Specification* (see Table 2).

4.2.1 Interrupt Configuration

In Figure 4-8, note the MPC8260A's additional sources for machine check interrupts. Also note that in addition to the internal sources, external pins, and CPM, the interrupt controller receives interrupts from the PCI bridge (MPC8265A and MPC8266A only) and TC layer (MPC8264A and MPC8266A only).

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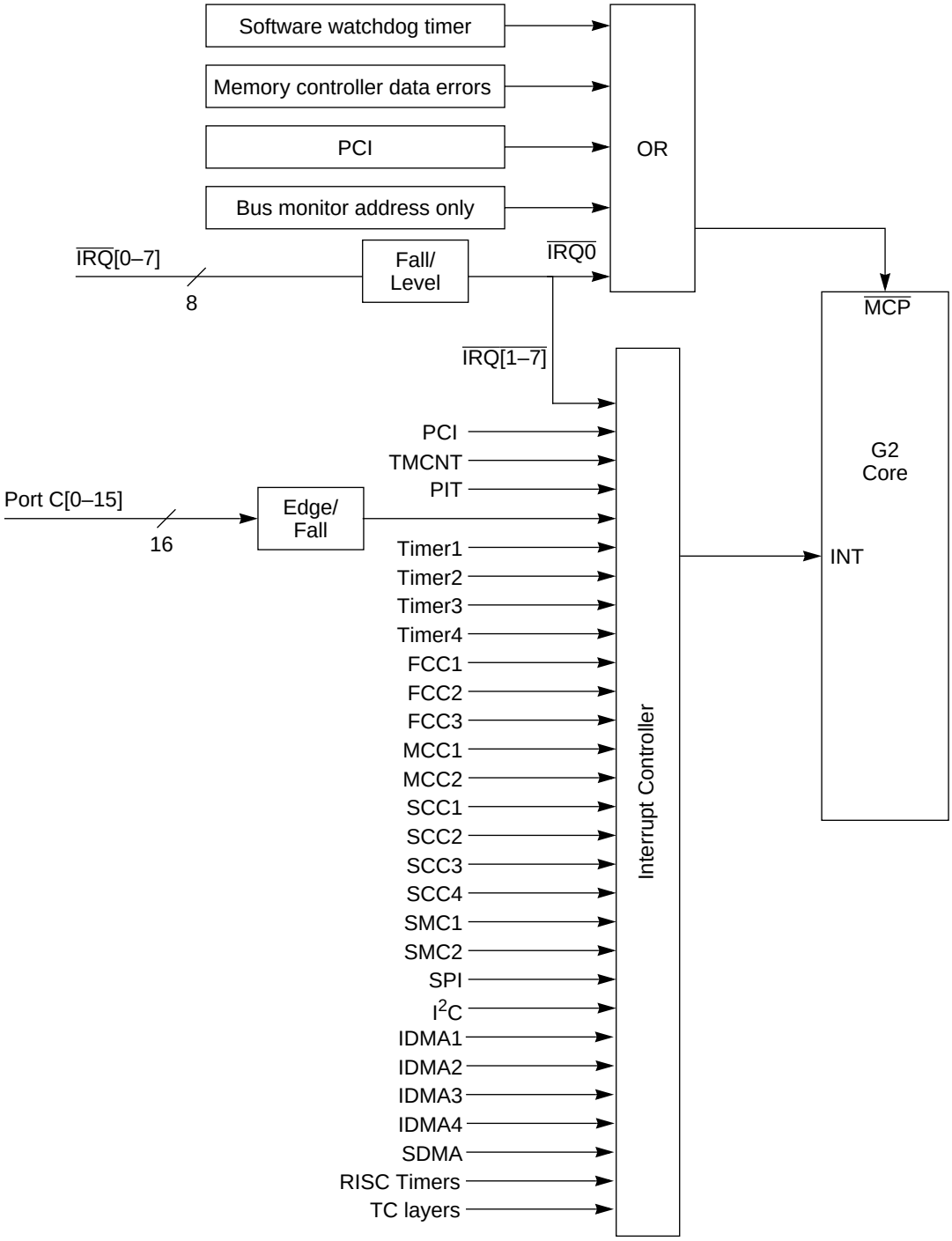

Figure 4-8. MPC8260A Interrupt Structure

4.2.1.1 (New) Machine Check Interrupt

There are several sources for a machine check interrupt:

- Software watchdog timer when programmed to generate an interrupt. See Section 4.1.5, “Software Watchdog Timer.”
- $\overline{\text{IRQ0}}$ signal when the internal core is enabled

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- Memory controller for parity/ECC errors. See Section 10.2.6, “Machine Check Interrupt (MCP) Generation.”
- PCI bridge (MPC8265A and MPC8266A only)
- Bus monitor time out on an address only transaction. See Section 4.1.1, “Bus Monitor.”

When the internal core is enabled, the MCP sources listed cause the interrupt controller to send a machine check interrupt to the core. When the core is disabled, the MCP assertion is reflected on $\overline{\text{IRQ0}}$/$\overline{\text{NMI_OUT}}$ so an external core can serve it.

4.2.1.2 (New) INT Interrupt

Besides the MCP sources, all other interrupts are taken by the core through the INT interrupt. If the internal core is disabled, INT is reflected on $\overline{\text{IRQ7}}$/$\overline{\text{INT_OUT}}$ so an external core can serve it.

The interrupt controller allows masking of each interrupt source. Multiple events within a CPM sub-block event are also maskable.

4.2.2 MPC8260A Interrupt Source Priorities

Table 4-3 shows prioritization of all the MPC8260A interrupt sources. The PCI bridge interrupt source is included in the XSIU locations and is discussed in *PCI Bridge Functional Specification*; the TC layer interrupt priority is configured with the SCCs in the YCC entries and is discussed in *TC Layer Functional Specification* (see Table 2). See Table 4-2 of the *MPC8260 User’s Manual* for more information on interrupt source priority levels.

4.2.4 MPC8260A Interrupt Vector Encoding

Table 4-3 lists the MPC8260A encodings (including the PCI bridge [MPC8265A and MPC8266A only] and the TC layer [MPC8264A and MPC8266A only]) for the six low-order bits of the interrupt vector.

Table 4-3. Encoding the Interrupt Vector

Interrupt Number	Interrupt Source Description	Interrupt Vector
0	Error (No interrupt)	0b00_0000
1	I^2C	0b00_0001
2	SPI	0b00_0010
3	RISC Timers	0b00_0011
4	SMC1	0b00_0100
5	SMC2	0b00_0101
6	IDMA1	0b00_0110
7	IDMA2	0b00_0111
8	IDMA3	0b00_1000
9	IDMA4	0b00_1001
10	SDMA	0b00_1010
11	Reserved	0b00_1011

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Table 4-3. Encoding the Interrupt Vector (Continued)

Interrupt Number	Interrupt Source Description	Interrupt Vector
12	Timer1	0b00_1100
13	Timer2	0b00_1101
14	Timer3	0b00_1110
15	Timer4	0b00_1111
16	TMCNT	0b01_0000
17	PIT	0b01_0001
18	PCI [1]	0b01_0010
19	IRQ1	0b01_0011
20	IRQ2	0b01_0100
21	IRQ3	0b01_0101
22	IRQ4	0b01_0110
23	IRQ5	0b01_0111
24	IRQ6	0b01_1000
25	IRQ7	0b01_1001
26–31	Reserved	0b01_1010–01_1111
32	FCC1	0b10_0000
33	FCC2	0b10_0001
34	FCC3	0b10_0010
35	Reserved	0b10_0011
36	MCC1	0b10_0100
37	MCC2	0b10_0101
38	Reserved	0b10_0110
39	Reserved	0b10_0111
40	SCC1	0b10_1000
41	SCC2	0b10_1001
42	SCC3	0b10_1010
43	SCC4	0b10_1011
44	TC layer[2]	0b10_1100
45–47	Reserved	0b10_1101–10_1111
48	PC15	0b11_0000
49	PC14	0b11_0001
50	PC13	0b11_0010
51	PC12	0b11_0011
52	PC11	0b11_0100
53	PC10	0b11_0101

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Table 4-3. Encoding the Interrupt Vector (Continued)

Interrupt Number	Interrupt Source Description	Interrupt Vector
54	PC9	0b11_0110
55	PC8	0b11_0111
56	PC7	0b11_1000
57	PC6	0b11_1001
58	PC5	0b11_1010
59	PC4	0b11_1011
60	PC3	0b11_1100
61	PC2	0b11_1101
62	PC1	0b11_1110
63	PC0	0b11_1111

[1] On MPC8265A and MPC8266A only. Reserved on other devices.

[2] On MPC8264A and MPC8266A only. Reserved on other devices.

4.3.2 MPC8260A System Configuration and Protection Registers

Although unchanged on the MPC8260A and so not included here, several registers include PCI-related additions. If using the MPC8265A or the MPC8266A, refer to the *PCI Bridge Functional Specification* (see Table 2).

4.3.2.1 Bus Configuration Register (BCR)

The bus configuration register (BCR), shown in Figure 4-21, contains configuration bits for various features and wait states on the 60x bus. Note the addition of the new field, SPAR (bit 26).

	0	1–3	4	5–7	8	9–10	11	12	13	14	15
Field	EBM	APD	L2C	L2D	PLDP	—	EAV	ETM	LETM	EPAR	LEPAR
Reset	Depends on reset configuration sequence. See Section 5.4.1, “Hard Reset Configuration Word.”										
R/W	R/W										

	16–18	19–20	21	22–25	26	27	28–31
Field	NPQM	—	EXDD	—	SPAR	ISPS	—
Reset	Depends on reset configuration sequence. See Section 5.4.1, “Hard Reset Configuration Word.”						
R/W	R/W						
Addr	0x10024						

Figure 4-21. Bus Configuration Register (BCR)

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Table 4-9 describes BCR fields.

Table 4-9. BCR Field Descriptions

Bits	Name	Description
0	EBM	Same as *MPC8260 Power QUICC II User's Manual*
1–3	APD	
4	L2C	
5–7	L2D	
8	PLDP	
9–10	—	
11	EAV	
12	ETM	
13	LETM	
14	EPAR	
15	LEPAR	
16–18	NPQM	
19–20	—	
21	EXDD	
22–25	—	
26	SPAR	Slave parity check. If set enables parity check on 60x bus transactions to the MPC8260A's internal memory space. In case of a parity error a core machine check is asserted and the error is reported in TESCR1[ISBE,PAR] and TESCR2[REGS,DPR,PCI0,PCI1,LCL].
27	ISPS	Same as *MPC8260 Power QUICC II User's Manual*
28–31	—	

4.3.2.10 MPC8260A 60x Bus Transfer Error Status and Control Register 1 (TESCR1)

The MPC8260A 60x bus transfer error status and control register 1 (TESCR1) is shown in Figure 4-31. Note the addition of the following fields: DER, IRQ0, SWD, and ADO (bits 20–23).

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	0	1	2	3	4	5	6	7	10	11	15
Field	BM	ISBE	PAR	ECC2	ECC1	WP	EXT	TC	—	TT	
Reset	0000_0000_0000_0000										
R/W	R/W										
Addr	0x10040										

	16	17	18	19	20	21	22	23	24	31
Field	—	DMD	—	PCIMCP[1]	DER	IRQ0	SWD	ADO	ECNT	
Reset	0000_0000_0000_0000									
R/W	R/W									
Addr	0x10042									

Figure 4-31. 60x Bus Transfer Error Status and Control Register 1 (TESCR1)

[1] MPC8265A, MPC8266A, MPC8250 only. Reserved on all other devices.

Table 4-15 describes TESCR1 fields.

Table 4-15. TESCR1 Field Descriptions

Bits	Name	Description
0	BM	Same as *MPC8260 Power QUICC II User's Manual*
1	ISBE	
2	PAR	
3	ECC2	
4	ECC1	
5	WP	
6	EXT	
7–9	TC	
10	—	
11–15	TT	
16	—	
17	DMD	
18	—	
19	PCIMCP	MPC8265A, MPC8266A, MPC8250 only (reserved on all other devices): PCI machine check. Set when a core machine check is asserted from the PCI bridge.
20	DER	Data error. Set when a core machine check is asserted due to ECC or parity errors.

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Table 4-15. TESCR1 Field Descriptions (Continued)

Bits	Name	Description
21	IRQ0	External machine check. Set when a machine check is asserted due to the external machine check pin (IRQ0).
22	SWD	Software watchdog time-out. Indicates that a core machine check was asserted due to a time-out in the software watchdog. See Section 4.1.5, “Software Watchdog Timer.”
23	ADO	60x bus monitor address-only time-out. Set when a core machine check is asserted due to time-out of the bus monitor in an address only transaction. See Section 4.1.1, “Bus Monitor.”
24–31	ECNT	Same as *MPC8260 Power QUICC II User’s Manual*

4.3.2.12 MPC8260A Local Bus Transfer Error Status and Control Register 1 (L_TESCR1)

The MPC8260A local bus transfer error status and control register 1 (L_TESCR1) is shown in Figure 4-33. Note the addition of the new field, DER (bit 20).

	0	1	2	3	4	5	6	7	9	10	11	15
Field	BM	—	PAR	—		WP	—	TC		—	TT	
Reset	0000_0000_0000_0000											
R/W	R/W											
Addr	0x10048											

	16	17	18	19	20	21	31
Field	—	DMD	—		DER	—	
Reset	0000_0000_0000_0000						
R/W	R/W						
Addr	0x1004A						

Figure 4-33. Local Bus Transfer Error Status and Control Register 1 (L_TESCR1)

The L_TESCR1 register bits are described in Table 4-17.

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Table 4-17. L_TESCR1 Field Descriptions

Bits	Name	Description
0	BM	Same as *MPC8260 Power QUICC II User's Manual*
1	—	
2	PAR	
3–4	—	
5	WP	
6	—	
7–9	TC	
10	—	
11–15	TT	
16	—	
17	DMD	
18–19	—	
20	DER	Data error. Set when a core machine check is asserted due to parity errors in the local bus.
21–31	—	Same as *MPC8260 Power QUICC II User's Manual*

MPC8260A Reset (Chapter 5)

Resetting the MPC8260A is the same as on the HiP3 MPC8260. However, with the addition of the PCI bridge on the MPC8265A and the MPC8266A, the local bus configuration options have been expanded to include its operation as the PCI bus (refer to the *PCI Bridge Functional Specification* (MPC8265AUMAD/D)).

60x Bus (Chapter 8)

8.4.3.2 Transfer Code Signals TC[0–2]

The transfer code signals, TC[0–2], provide supplemental information about the corresponding address (primarily regarding the source of the transaction). Note that TC*x* signals can be used with the TT[0–4] and $\overline{\text{TBST}}$ to further define the current transaction.

Table 8-3. Transfer Code Encoding

TC[0–2]	60x Bus		Local Bus
	Read	Write	
000	Core data transaction	Any write	60x-local bridge
001	Core touch load	—	Reserved
010	Core instruction fetch	—	Local DMA function code 0
011	Reserved	—	Local DMA function code 1

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Table 8-3. Transfer Code Encoding (Continued)

TC[0–2]	60x Bus		Local Bus
	Read	Write	
100	PCI bridge transaction		Reserved
101	Reserved		
110	DMA function code 0		
111	DMA function code 1		

Communications Processor Module Overview (Chapter 13)

Major new CPM features in MPC8260A are as follows:

- 32-Kbyte dual-port RAM
- Additional MCC host commands

13.3.6 MPC8260A RISC Controller Configuration Register (RCCR)

The MPC8260A RISC controller configuration register (RCCR), shown in Figure 13-3, has an expanded ERAM field to accommodate the expanded dual-port RAM.

	0	1	2–7	8	9	10–11	12	13	14–15
Field	TIME	MCCPR	TIMEP	DR1M	DR2M	DR1QP	EIE	SCD	DR2QP
Reset	0000_0000_0000_0000								
R/W	R/W								
Addr	0x119C4								

	16–19	20	21	22	23	24	25	26–27	28	29	30–31
Field	ERAM	EDM1	EDM2	EDM3	EDM4	DR3M	DR4M	DR3QP	DEM12	DEM34	DR4QP
Reset	0000_0000_0000_0000										
R/W	R/W										
Addr	0X119C6										

Figure 13-3. RISC Controller Configuration Register (RCCR)

MPC8260A RCCR bit fields are described in Table 13-3. Note that RCCR fields not shown below are unchanged.

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Table 13-3. RISC Controller Configuration Register Field Descriptions

Bits	Name	Description
0	TIME	Same as *MPC8260 Power QUICC II User's Manual*
1	MCCPR	
2–7	TIMEP	
8, 9, 24, 25	DR*x*M	
10–11, 14–15, 26–27, 30–31	DR*x*QP	
12	EIE	
20, 21, 22, 23	EDM*x*	
28	DEM12	
29	DEM34	
13	SCD	Scheduler configuration. Configure as instructed in the download process of a Motorola-supplied RAM microcode package. 0 Normal operation 1 Alternate configuration of the scheduler, according to bit 19 (in the ERAM field): If RCCR[19] = 0, the jump table starts at dual-port RAM address 0x0000. If RCCR[19] = 1, the jump table starts at dual-port RAM address 0x4000.
16–19	ERAM	Enable RAM microcode. Configure as instructed in the download process of a Motorola-supplied RAM microcode package. 0000 Disable microcode program execution from the dual-port RAM. (That is, microcode execution starts at ROM address 0x0000 after reset.) In the following configurations, microcode execution starts at RAM address 0x0000 after reset: 0010 Microcode uses the first 2 Kbytes of the dual-port RAM + 8 Kbytes starting from 0x4000. 0100 Microcode uses the first 4 Kbytes of the dual-port RAM + 8 Kbytes starting from 0x4000. 0110 Microcode uses the first 6 Kbytes of the dual-port RAM + 8 Kbytes starting from 0x4000. 1000 Microcode uses the first 8 Kbytes of the dual-port RAM + 8 Kbytes starting from 0x4000. 1010 Microcode uses the first 10 Kbytes of the dual-port RAM + 8 Kbytes starting from 0x4000. 1100 Microcode uses the first 12 Kbytes of the dual-port RAM + 8 Kbytes starting from 0x4000. In the following configurations, microcode execution starts at RAM address 0x4000 after reset: 0011 Microcode uses 2 Kbytes starting from dual-port RAM address 0x4000. 0101 Microcode uses 4 Kbytes starting from dual-port RAM address 0x4000. 0111 Microcode uses 6 Kbytes starting from dual-port RAM address 0x4000. 1001 Microcode uses 8 Kbytes starting from dual-port RAM address 0x4000. Note that all other configurations not listed are reserved.

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13.4.1.1 MPC8260A CP Commands

Table 13-7 shows the MPC8260A's additional CP command opcodes for the MCCs.

Table 13-7.CP Command Opcodes

Opcode	Channel									
	FCC	SCC	SMC (UART/ Transparent)	SMC (GCI)	SPI	I^2C	IDMA	MCC	Timer	Special
0011	ENTER HUNT MODE	ENTER HUNT MODE	ENTER HUNT MODE	—	—	—	—	INIT RX AND TX PARAMS (one channel)	—	—
0101	GRACEFUL STOP TX	GRACEFUL STOP TX	—	—	—	—	—	INIT TX PARAMS (one channel)	—	—
0110	RESTART TX	RESTART TX	RESTART TX	—	—	—	—	INIT RX PARAMS (one channel)	—	—
0111	CLOSE RX BD	CLOSE RX BD	CLOSE RX BD	—	CLOSE RX BD	CLOSE RX BD	—	MCC RESET	—	—

Table 13-8 describes the additional MPC8260A commands listed in Table 13-7; all other commands are unchanged and are described in the *MPC8260 User's Manual*.

Table 13-8. Command Descriptions

Command	Description
INIT MCC RX AND TX PARAMS — ONE CHANNEL	Initialize receive and transmit parameters. Initializes the receive and transmit parameters of the peripheral controller. Differs from INIT RX AND TX PARAMS in that, for the MCCs, issuing INIT RX AND TX PARAMS initializes 32 consecutive channels beginning with the channel number specified in CPCR[MCN], but issuing INIT MCC RX AND TX—ONE CHANNEL initializes only the channel in the command; see Section 27.9, "MCC Commands."
INIT MCC RX PARAMS— ONE CHANNEL	Initialize MCC receive parameters for only a single channel according to MCC channel number field. See Section 27.9, "MCC Commands."
INIT TX PARAMS— ONE CHANNEL	Initialize MCC transmit parameters for only a single channel according to MCC channel number field. See Section 27.9, "MCC Commands."
MCC RESET	MCC reset. Provides a hard reset to the MCC FIFOs. See Section 27.9, "MCC Commands." To use this command, software should execute the following sequence: 1 Disable the TDM by clearing the appropriate enable bit in SIxGMR[4-7] (See Table 14-4, "SIxGMR Field Descriptions."). 2 Issue the MCC RSET command. 3 Issue the INIT RX AND TX command. 4 Reprogram the specific MCC channel, global parameters, and any BDs that need to be updated. 5 Set the appropriate enable bit in SIxGMR[4-7]. (See Table 14-4, "SIxGMR Field Descriptions.").

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13.5 MPC8260A Dual-Port RAM

The dual-port RAM on the MPC8260A has been expanded to 32 Kbytes of static RAM. An extra 8 Kbytes starting at address 0x4000 is available for microcode execution only and cannot be used for data buffers or BDs. However, when not used for microcode, the extra 8 Kbytes can be accessed from the 60x bus for general purpose internal storage. Figure 13-8 shows the MPC8260A memory map of the dual-port RAM.

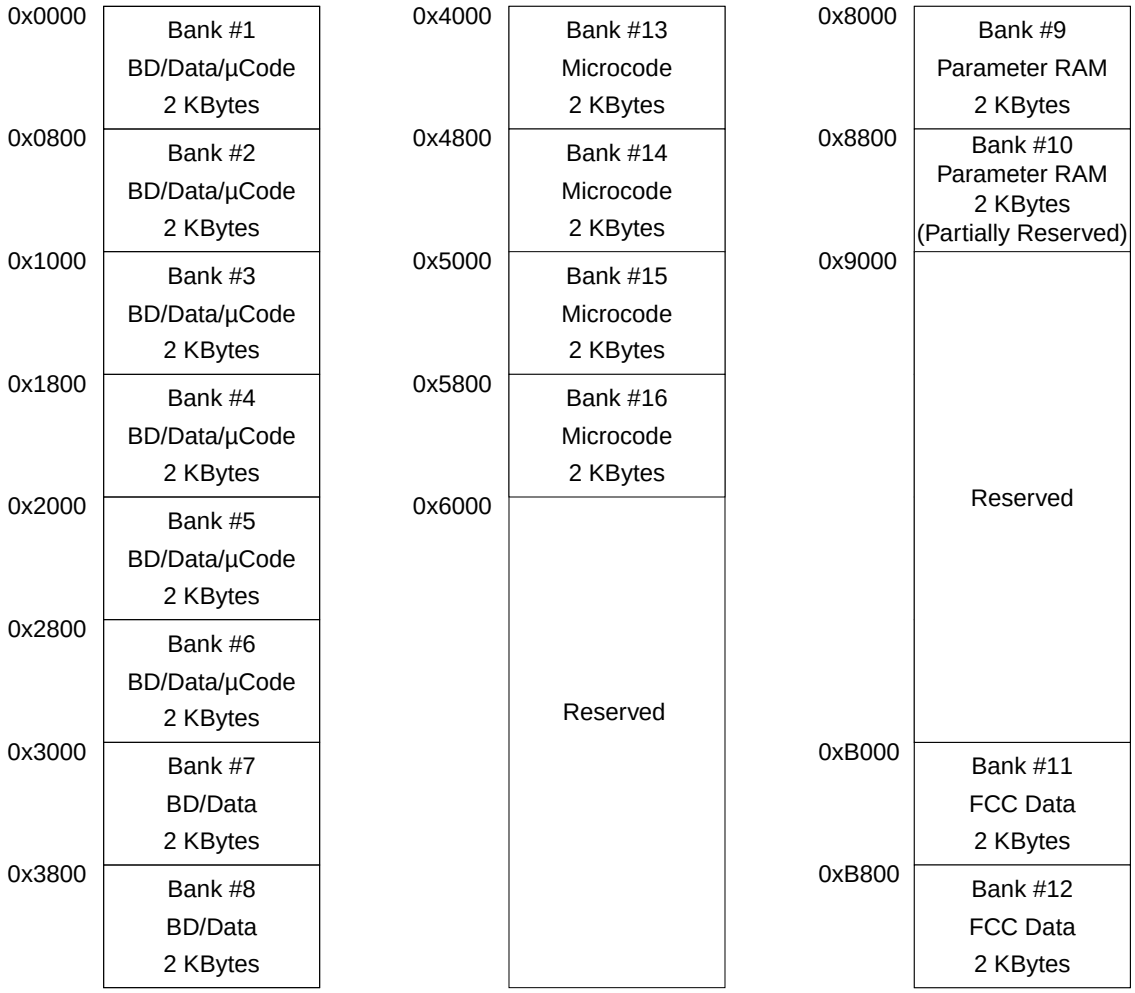

Figure 13-8. MPC8260A Dual-Port RAM Memory Map

Parallel I/O Ports (Chapter 35)

The MPC8260A parallel I/O ports are the same as the MPC8260 with the exception of the following secondary pin options:

- FCC1: RxPrty UTOPIA
- FCC1: TxPrty UTOPIA
- SPI: $\overline{\text{SPISEL}}$
- SPI: SPICLK

The following sections show the MPC8260A modifications to ports A, C, and D.

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35.5.1 MPC8260A Port A Modifications

Table 35-5 shows the MPC8260A modifications for the port A pin assignments.

Table 35-5. MPC8260A Port A—Dedicated Pin Assignment (PPARA = 1)

Pin	Pin Function					
	PSORA = 0			PSORA = 1		
	PDIRA = 1 (Output)	PDIRA = 0 (Input)	Default Input	PDIRA = 1 (Output)	PDIRA = 0 (Input, or Inout if Specified)	Default Input
PA5	**SCC2: $\overline{\text{RSTRT}}$**	**FCC1: RxPrty**[1] UTOPIA (secondary option)	GND	**FCC2: RxAddr[2]** MPHY master	**IDMA4: DREQ**	GND

[1] Available only when the primary option for this function is not used.

35.3 MPC8260A Port C Modifications

Table 35-7 shows the MPC8260A modifications for the port C pin assignments.

Table 35-7. MPC8260A Port C Dedicated Pin Assignment (PPARC = 1)

PIN	Pin Function					
	PSORC = 0			PSORC = 1		
	PDIRC = 1 (Output)	PDIRC = 0 (Input)	Default Input	PDIRC = 1 (Output)	PDIRC = 0 (Input or Inout if Specified)	Default Input
PC22	**FCC1: TxPrty** UTOPIA (secondary option)[1]	CLK10	CLK14		**IDMA1: $\overline{\text{DONE}}$** Inout (primary option)	by PD5
PC19	**BRG7: BRGO**	CLK13	GND		**SPI: SPICLK**[1] Inout (secondary option)	GND
PC16		CLK16/TIN4	GND			
PC1	**BRG6: BRGO**	**IDMA2: DREQ**	GND	**TDM_A2: $\overline{\text{L1RQ}}$**	**SPI: $\overline{\text{SPISEL}}$**[1] (secondary option)	V_{DD}

[1] Available only when the primary option for this function is not used.

35.4 MPC8260A Port D Modifications

Table 35-8 shows the MPC8260A modifications for the port D pin assignments.

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Table 35.8. MPC8260A Port D Dedicated Pin Assignment (PPARD = 1)

Pin	Pin Function					
	PSORD = 0			PSORD = 1		
	PDIRD = 1 (Output)	PDIRD = 0 (Input)	Default Input	PDIRD = 1 (Output)	PDIRD = 0 (Input, or Inout if Specified)	Default Input
PD19	**FCC1: TxAddr[4]** MPHY, master, multiplexed polling **FCC2: TxAddr[3]** MPHY, master, multiplexed polling	**FCC1: TxAddr[4]** MPHY, slave, multiplexed polling **FCC1: TxClav3** MPHY, master, direct polling **FCC2: TxAddr[0]** MPHY, slave, multiplexed polling	GND	**BRG1: BRGO**	**SPI: $\overline{\text{SPISEL}}$** (primary option)	PC1
PD18	**FCC1: RxAddr[4]** MPHY, master, multiplexed polling **FCC2: RxAddr[3]** MPHY, master, multiplexed polling	**FCC1: RxAddr[4]** MPHY, slave, multiplexed polling **FCC1: RxClav3** MPHY, master, direct polling **FCC2: RxAddr[0]** MPHY, slave, multiplexed polling	GND		**SPI: SPICLK** Inout (primary option)	PC19
PD17	**BRG2: BRGO**	**FCC1: RxPrty** UTOPIA (primary option)	PA5		**SPI: SPIMOSI** Inout	V_{DD}
PD16	**FCC1: TxPrty** UTOPIA (primary option)	**TDM_C1: L1TSYNC/GRANT** (secondary option)	GND		**SPI: SPIMISO** Inout	SPI MOSI

Document Revision History

Document Revision History

Document Revision	Substantive Changes
0	Initial version
0.1	Table 3-1: DLLMR and DLLST have been removed. Internal address 10C98–10CFF is reserved. **Nontechnical changes** • Organizational. Removal of PCI-specific and TC -layer-specific information that is not pertinent to the MPC8260A (this information can be found in the relevant documents mentioned in Table 2). • Removal. Information unchanged by HiP4 enhancements has been removed (from the memory map, for instance). This information can be found in the *MPC8260 PowerQUICC II User's Manual.* • Numbering. Section, figure, and table numbering have been changed to correspond to the *MPC8260 PowerQUICC II User's Manual.*

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